

Berg
Serial no. 10/045,927
Filed 1/9/2002
Attorney docket no. BEA920000017US1

Page 5

REMARKS

Status of and amendment to claims

Claims 1-9 are pending in the patent application. Claims 1, 2, and 8 are independent claims, from which the remaining pending claims ultimately depend. Each of the independent claims has been amended so that state information is stored "exclusively" within the interconnect connecting the nodes of the multiprocessor system to one another, "such that the interconnect is a sole repository of cache coherence information" within the system.

Applicant submits that the amendments made to the independent claims are at least inherently supported by the specification of the patent application as originally filed. As a whole, the patent application only discloses the interconnect (such as the crossbar system 70/72) as storing state information, such that it is the sole repository of cache coherence information within the system. For instance, an object of the present invention is "to provide a system for maintaining coherence of data stored in multiple caches located in separate nodes within a multi-node multiprocessor system *which utilizes a data tag and address crossbar control and communications device.*" (P. 5, ll. 17-20) That is, there are no other devices, mechanisms, or components within the system disclosed in the specification that maintain cache coherence information of data stored in caches located in the nodes of the system.

Applicant notes that the MPEP states that "[t]he subject matter of [a] claim need not be described literally (i.e., using the same terms or *in haec verba*) in order for the disclosure to satisfy the description requirement." (MPEP sec 2163.02) The MPEP further notes that

By disclosing in a patent application a device that inherently performs a function *or has a property*, operates according to a theory or has an advantage, a patent application necessarily discloses that function, theory or advantage, even though it says nothing *explicit* concerning it. The application may later be amended to recite the function, theory or advantage without introducing prohibited new matter.

Berg
Serial no. 10/045,927
Filed 1/9/2002
Attorney docket no. BEA920000017US1

Page 6

(MPEP sec. 2163.07(a) (citations omitted) (emphasis added)) Thus, it is completely proper for Applicant to amend the claims to include limitations that are not literally described in the patent application, where such limitations are inherent to that which is being claimed.

Claim rejections under 35 USC 102(b)

Claims 1-9 have been rejected as being anticipated by Luick (6,088,769). Applicant submits that as amended, independent claims 1, 2, and 8 are not anticipated by Luick, such that all of the pending claims are patentable over Luick.

Luick specifically discloses utilizing both local tables within the nodes of a microprocessor system, as well as a global table within an interconnect of a microprocessor system, to store cache coherence information. The title of Luick itself indicates that its invention is directed to “multiprocessor cache coherence *directed by combined local and global tables*.” Each node in particular has a local coherence unit, such that “[e]ach local coherence unit maintains a table which indicates whether the most current copy of data stored within the node resides in the local memory . . . , in the local cache . . . , or in a non-local cache” (Col. 2, ll. 34-41) Thus, Luick cannot anticipate the claimed invention, in which information regarding the state of data is stored “exclusively” within the interconnect, where “the interconnect is a sole repository of cache coherence information” within the system.

Furthermore, Luick cannot be modified to render the claims unpatentable as obvious over Luick under 35 USC 103. Luick indicates that maintaining one coherence table is undesirable, because it “increases the complexity and width of directory entries within such tables, making the table relatively large and complex.” (Col. 1, l. 66, through col. 2, l. 2) An object of the invention of Luick is thus “to provide a system and method for maintaining coherence of data stored in multiple caches within a multiprocessor system by storing relatively small and simple entries in coherence tables.” (Col. 2, ll. 3-7) Luick achieves this by “[t]he use of local coherence tables *and*

Berg
Serial no. 10/045,927
Filed 1/9/2002
Attorney docket no. BEA920000017US1

Page 7

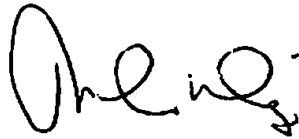
a global coherence table," which "reduces the size and complexity of the coherence table that would otherwise be required." (Col. 3, ll. 7-9)

Thus, in the first instance, Luick teaches away from having a sole repository of cache coherence information, indicating that using a single table is undesirable, such that there is no motivation to modify Luick to have such a sole repository. Furthermore, in the second instance, Luick's stated purpose and object of storing relatively small and simple entries in multiple coherence tables is achieved by using both local and global tables, so modifying Luick to have a sole repository to store cache coherence information would destroy its intended purpose and object, such that modifying Luick to have a sole repository of such information is improper. In sum, therefore, Luick neither anticipates the claimed invention nor renders it obvious.

Conclusion

Applicants have made a diligent effort to place the pending claims in condition for allowance, and request that they so be allowed. However, should there remain unresolved issues that require adverse action, it is respectfully requested that the Examiner telephone Applicants' Attorney so that such issues may be resolved as expeditiously as possible. For these reasons, this application is now considered to be in condition for allowance and such action is earnestly solicited.

Respectfully Submitted,



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Date

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